IDEC Chip Design Contest

# A 900μW, 1-4GHz Input-Jitter-Filtering Digital-PLL-Based 25%-Duty-Cycle Quadrature-Clock Generator for Ultra-Low-Power Clock Distribution in High-Speed DRAM Interfaces

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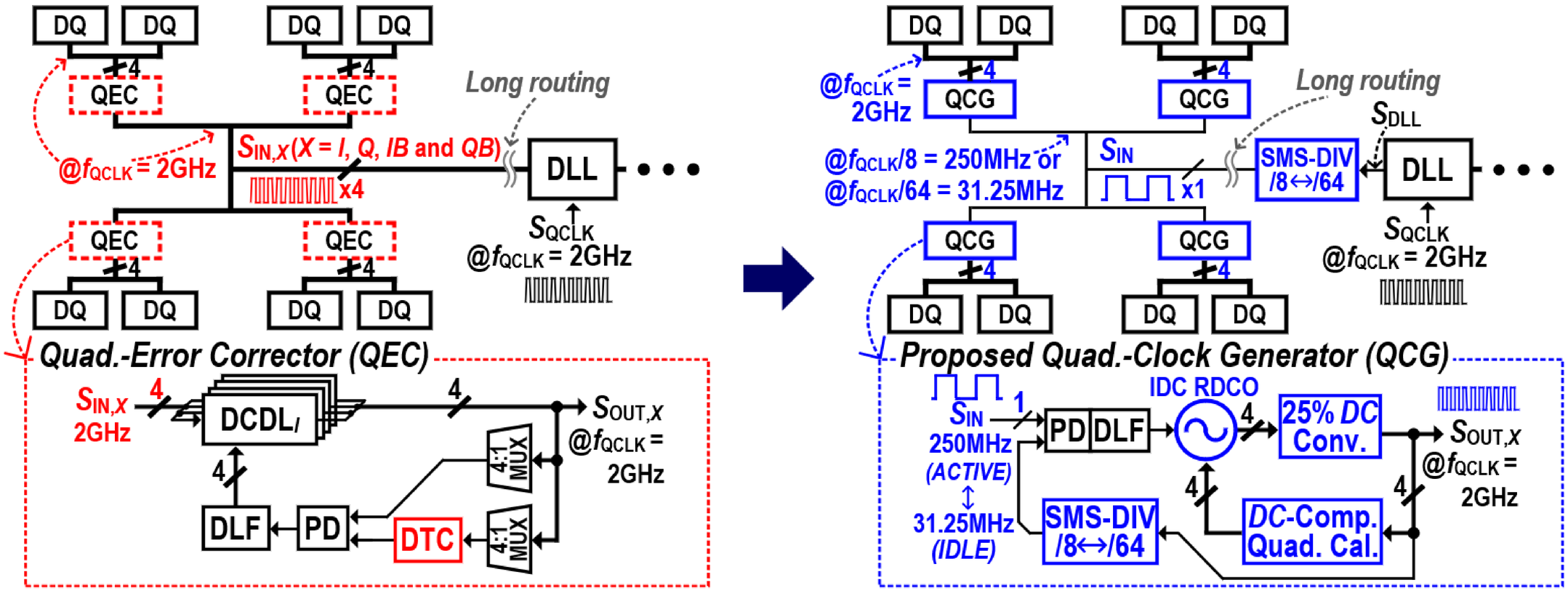
## Conv. Clock-Dist. and Proposed Low-Power Clock Dist. w/ Quad.-Clock Generator (QCG)

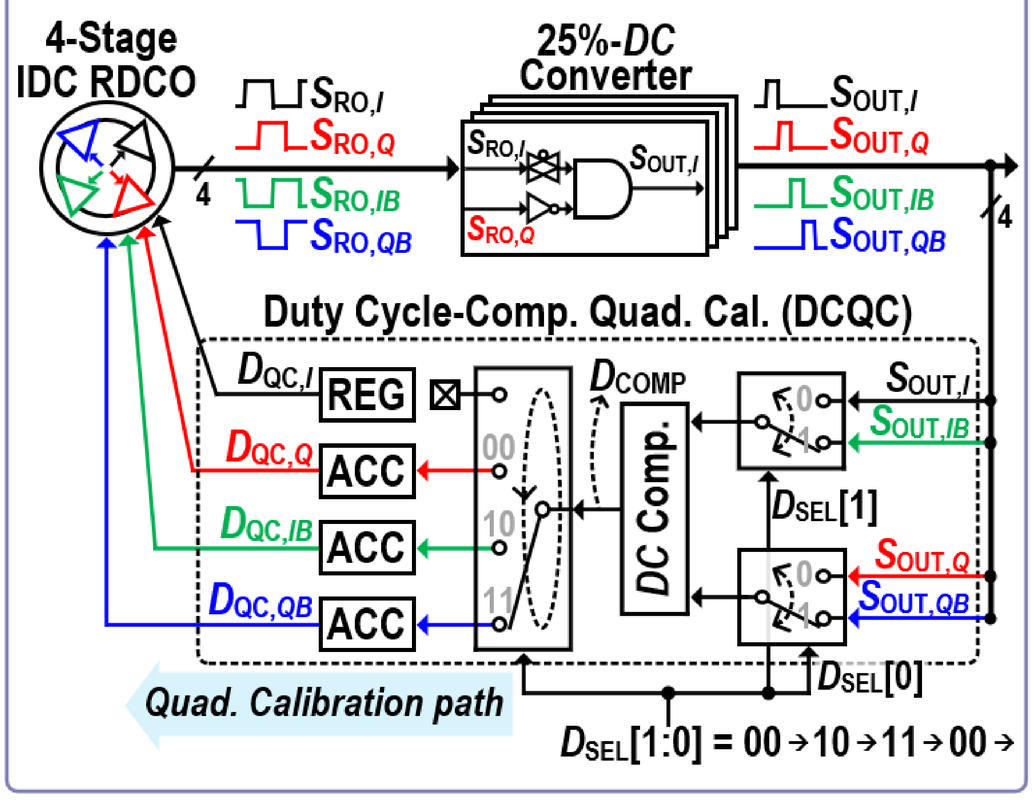



☺ Distribute single-phase clock at a lower frequency → Ultra-low power consumption

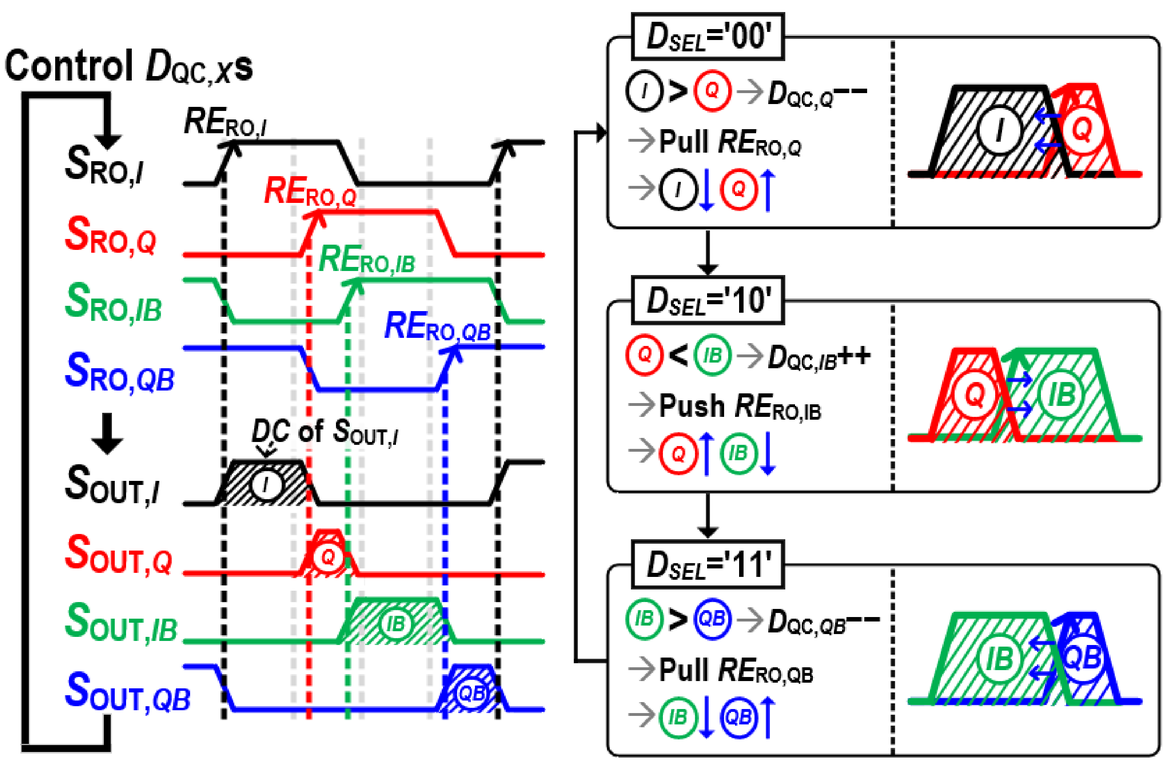
☺ Digital PLL (DPLL)-based QCG → Input-jitter filtering & Precise 25% Duty-Cycle (*DC*)

## Overall Architecture of Proposed QCG and Operation of DCQC

### Architecture of QCG



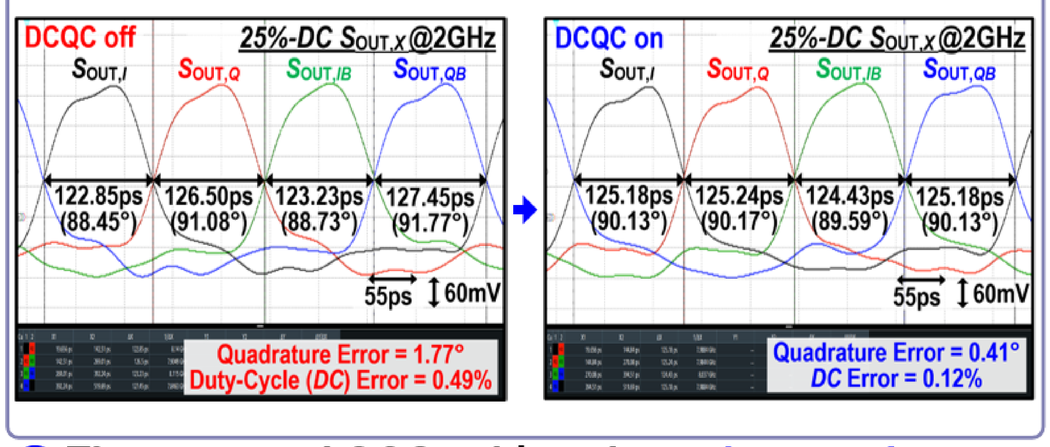

### Operation of DCQC




- DCQC corrects quad. errors by controlling each delay cell of the Individual-Delay-Controlling Ring DCO (IDC RDCO).
- 4 output signals do not overlap one another → An equal 25% *DC* can guarantee the precise quad. relationship.

## Measurement Results and Performance Comparison

### Waveforms




| | This work | ISSCC'20 [1] | TCASII'17 [2] | TVLSI'19 [3] | ESSCIRC'21 [4] | JSSC'21 [5] |
|---|---|---|---|---|---|---|
| Process | 40nm | 40nm | 65nm | 55nm | 28nm | 28nm |
| Architecture | Digital-PLL QCG | Digital-DLL QEC | Digital-DLL QEC | Digital-DLL QEC | Digital-DLL QEC | Digital-DLL QCG |
| Quadrature Clock | Gen./ Correc. | Correc. | Correc. | Correc. | Correc. | Gen./ Correc. |
| **Duty-Cycle (*DC*)** | **25% & 50%** | **50%** | **50%** | **50%** | **50%** | **50%** |
| **Freq. ($f_{QCLK}$) Range** | **1.0 – 4.0GHz** | **0.8 – 2.3GHz** | **1.25GHz** | **1.0 – 3.0GHz** | **0.8 – 3.2GHz** | **1.3 – 4.0GHz** |
| **Jitter Filtering** | **Yes** | **No** | **No** | **No** | **No** | **No** |
| **Input → Output Jitter$_{rms}$ @$f_{QCLK}$** | **2.94ps→1.22ps @2.0GHz** | **2.28ps→2.34ps @2.3GHz** | **1.84ps→2.53ps @1.25GHz** | **1.85ps→2.14ps @3.0GHz** | **NA*→1.31ps @3.2GHz** | **0.96ps→1.82ps @4.0GHz** |
| **Quadrature Error** | **< 0.5°** | **< 2.18°** | **< 0.48°** | **< 1.11°** | **< 1.84°** | **< 2.82°** |
| **Power Cons. @$f_{QCLK}$** | **0.9mW@2.0GHz** | **8.9mW@2.3GHz** | **2.3mW@1.25GHz** | **2.1mW@3.0GHz** | **9.80mW@3.2GHz** | **6.5mW@4.0GHz** |
| **Power Efficiency** | **0.45mW/GHz** | **3.87mW/GHz** | **1.82mW/GHz** | **0.69mW/GHz** | **3.06mW/GHz** | **1.63mW/GHz** |
| Active Area | 0.011mm$^2$ | 0.012mm$^{2**}$ | 0.004mm$^{2**}$ | 0.003mm$^2$ | 0.010mm$^2$ | 0.004mm$^2$ |

☺ The proposed QCG achieved very low quad. errors over the largest freq. range while consuming lowest power

**Reference** [1] S. Shin et al., *ISSCC*, pp.340-342, 2020. [2] Y. Kim et al., *IEEE TCAS-II*, vol. 64, no.4, pp.397-401, April 2017. [3] J. Chae et al., *IEEE Tran. VLSI*, vol. 27, no. 4, pp. 978-982, April 2019. [4] H. Yoon et al., *ESSCIRC*, pp. 463-466, Sept. 2021. [5] H. Park et al., *IEEE JSSC*, vol. 56, no. 6, pp. 1886-1896, June 2021.

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